

Abstract of the Disclosure:

A clock configuration for driving switched op-amp circuits operated in opposite phases is presented in which a common off-phase of variable length is inserted between the on-phases  
5 of the individual operational amplifiers. The length of the off-phase can be adapted to the transient response of the operational amplifiers used. The clock configuration according to the invention can be used for further reducing the power consumption of switched op-amp circuits.

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